On Clock Network Design for Sub-threshold Circuitry

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***Abstract*—In this paper, we introduce the clock network design challenge for sub-threshold(sub-V_T) circuits and summarize several proposed clock network topologies for sub-V_T from related work. Specifically, a review of clock network design challenges and their manifestation in sub-V_T is given. We summarize the results of related work regarding a clock slew control circuit technique, a proposed clock buffer for sub- V_T, and clock tree topology discussions for sub-V_T. We evaluate the effectiveness of each methodology through metrics that characterize clock distribution networks such as slew, skew, and power consumption, and identify the scope and limitations of the proposed solutions.**

***Index Terms*— Clock distribution network, Robust design, Sub-threshold circuits**

I. Introduction

Sub-threshold(sub-V_T) circuit operation has become increasingly attractive for applications where energy is constrained or low power consumption is the main focus. Such applications include portable electronics and biomedical sensor nodes[1]. Quadratic savings in dynamic energy and power are achieved through supply voltage scaling, and thus substantial power and energy may be saved by scaling to sub-V_T voltages[2][3].

However, sub-V_T operation poses problems to the clock network design of digital circuits. Namely, due to transistor delay's exponential dependency on the value of the transistor threshold voltage V_{th}, sub-V_T clock networks are sensitive to process variations. Also, current and drive strength for clock buffers are orders of magnitude lower than super-threshold operation. These setbacks in sub-V_T in turn compromise the robustness of sub-V_T clock networks, leading to problems such as unacceptable levels of clock slew and skew. For example, it has been stated in [4] that uncontrolled clock slew may cause up to 90% deterministic fluctuation in timing parameters such as setup time and hold time. To exacerbate the problem, conventional super-threshold solutions to these problems, such as excessive buffering in the clock distribution network to control skew, are not suitable in sub-V_T(because the clock buffers themselves exhibit exponentially varying delay). In other cases, extra design efforts, such as gate upsizing or using clock grids to increase the circuits' robustness to process variation and low drive, require great increases in power consumption, undermining our purpose of low power. As the clock network may consume 40% of the circuit's total dynamic power[5], clearly, designing a robust, low power clock network is a vital task for sub-V_T circuits.

II. Background for Clock Networks in Sub-VT

A. Timing and Clock Networks

To understand the importance of a robust clock network for digital circuits, we need only to observe the timing constraint equations that apply to all logic paths.

$$T_{CLK} + \delta \geq t_{c-q}(t_{slew}) + t_{\log ic} + t_{su}(t_{slew}) \quad (1)$$

$$t_{hold}(t_{slew}) + \delta < t_{c-q,cd} + t_{\log ic,cd} \quad (2)$$

As can be seen, both skew and slew, which are imperfections in the clock distribution network, have implications on timing constraints. Specifically, the setup constraint, or equation (1), becomes harder to meet in the presence of negative skew and clock slew. Both $t_{c\text{-}q}$ and t_{su} are functions of clock slew, and increase with increasing slew. Similarly, equation (2), or the hold constraint, becomes harder to meet with positive skew and large slew.

B. Conventional Clock Network Design and Shortcomings in Sub-threshold

The purpose of local clock distribution schemes is to deliver a sharp clock signal(minimal slew) with as little phase difference possible(minimal skew) to the registers in the circuit design. A common topology used is the H-tree, where numerous clock buffers are laid out so that the signals produced by groups of clock buffers at the same distance from the clock source (same 'level' of clock tree) ideally have identical timing characteristics. A conceptual diagram of an H-tree is given in Fig.. The key in this configuration is that the clock buffers are sized and spaced so that not only do they provide drive strength at the registers(slew control), the delay through each path is equivalent(skew control).

However, this and many other conventional super-threshold topologies fail to address issues arising from sub-threshold operation that undermine the generation of a robust clock signal. As can be seen from the current equation for a transistor operating in sub-V_T, there is an exponential dependency for the current, and thus the gate delay, on $V_{th.}$

$$I_D = I_o \frac{W}{L} 10^{(V_{gs}-V_{th}+\eta V_{ds})/s}(1-e^{-V_{ds}/V_{th}}) \quad (3)$$

Thus, transistors are very much suspect to process variations. The delay through different clock paths may vary greatly, causing great amounts of skew, even if the paths were balanced schematically. What's more, typical sub-V_T current levels are $10^3\times$ less than in super-threshold, meaning the clock

buffers directly driving the registers have drastically slower slew rates than their super-threshold counterparts that compromise the timing robustness of the circuit.

Recognizing the insufficiencies of conventional clock networks, we summarize different proposed approaches in the following sections.

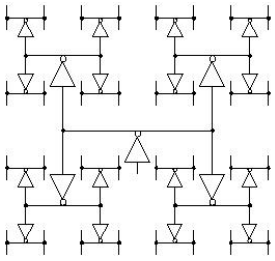

Fig. 1. Conventional H-tree topology. Buffer at middle represents clock source. Registers not shown at end of un-buffered lines.

III. Energy and Slew Aware Clock Design

In the work of [4], a clock network methodology is proposed where the constraint on the load of the clock buffers for each level of the tree are carefully analyzed to control slew for sub-V_T circuits. As mentioned in Section II, poor slew leads to degradation to timing margins as it affects $t_{c\text{-}q}$, $t_{su,}$ and $t_{hold.}$

It was stated in [4] that slew variations can cause up to 90% degradation in setup, clock-to-q, and hold time for a conventional clock tree designed in super-threshold scaled to operate in sub-V_T. The setup time deterministic variation as an example is given in Fig. (a). A keen observation leads insight into how slew can be controlled without sacrificing low power. Depicted in Fig. (b), we notice that slew recovery is a strong function of nodal load capacitance. Thus, the authors of [4] proposed a dynamic nodal capacitance technique that puts limits on the maximum capacitance C_{MAX} a buffer can drive, allowing larger slew at early levels of the clock tree but stringent constraint on slew at levels near the registers. This is in contrast to a conventional clock tree that has a fixed C_{MAX} constraint on all nodes.

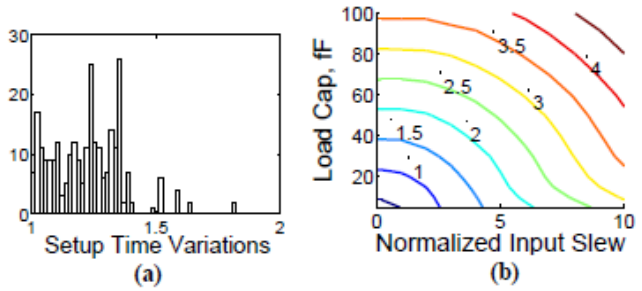

Fig. 2. [4](a) Deterministic setup time variations for a conventional clock tree in sub-vt. (b) Output slew contours with regards to input slew and output node load capacitance.

Since gate capacitance is one of the main contributors to nodal capacitance, there is a tradeoff between slew control and power consumption of the clock network. A loose C_{MAX} constraint on a buffer implies a buffer may have a higher fan-out, requiring less buffers in the ensuing clock level, meaning less power consumption but greater slew. A tightly constrained C_{MAX} is vice versa. Therefore, this technique translates itself to determining how much fan-out different buffers should be allowed to drive, with looser C_{MAX} near the clock source and tight C_{MAX} near the registers.

Optimal results in the sense where slew is controlled without sacrificing low power(the designed clock tree consumes 3% less power compared to the conventional base case tree) are shown in Fig. 3(a). The technique is able to contain slew and thus setup time design distribution, and is more robust to process variations. It is also interesting to see that this technique contributes to reducing skew as well. This is because with looser C_{MAX} at initial levels, there are fewer buffers in the levels close to the clock source, meaning a smaller chance for imbalanced paths. Clearly, this is an effective method in controlling slew for sub-V_T clock networks.

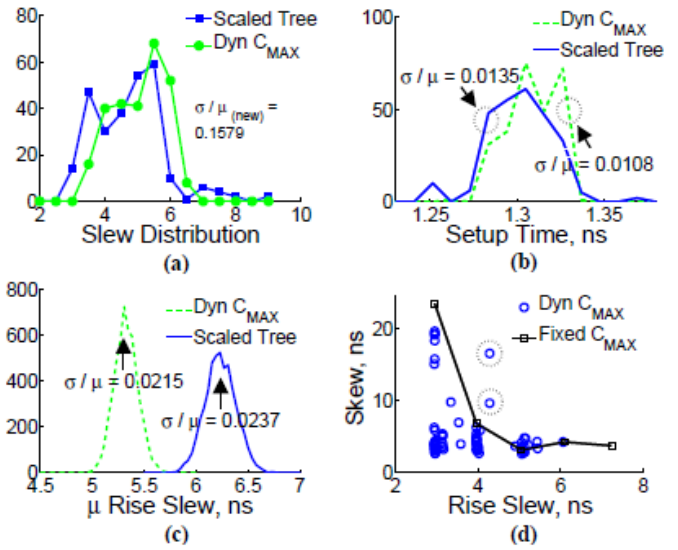

Fig. 3. [4]Results for slew control technique showing better (a) slew distribution in design, improved (b) setup time distribution, and robustness to (c) process variations. It is interesting to see that this technique indirectly helps (d) clock skew as well.

IV. High-Speed Variation Tolerant Clock Buffer Design for Sub-Threshold

As described, it is the imperfections in the clock buffers of weak drive for sub-V_T and subjectivity to process variation that lead to poor clock networks. Therefore, another approach is to re-design the clock buffer in a way tolerant to these shortcomings. [6] looks into this approach, and a novel circuit using capacitive boosting is proposed.

For brevity, its operation and design will not be described in length, but in principle, by increasing the gate voltage of the driving transistors in the buffer through capacitive boosting, the transistors' operating region is shifted into super-threshold. This not only enhances performance with much smaller slew rates, but super-threshold operation rids the transistors of exponential effects of process variations. The concept of boosting is shown in Fig. 4. This is attractive in sub-V_T where current is an exponential function of V_{gs}. Using this clock buffer, the clock tree designed exhibits 66% reduction in 3σ skew, and 2.5× faster slew rates. However, this circuit has certain drawbacks. Specifically, it incurs a half cycle pre-charge startup penalty and is not readily integrated into digital

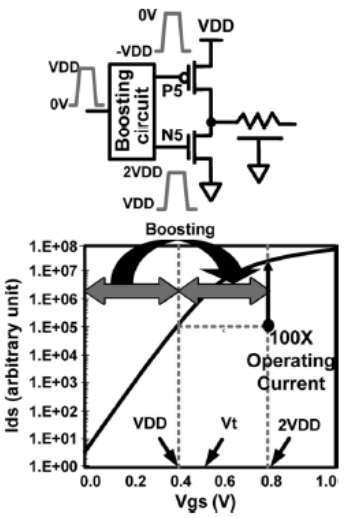

Fig. 4. [6]Conceptual diagram of capacitive boosting and current dependency on gate voltage.

design flows. Leakage current is greatly increased and may undermine our purposes of low power. In fact, it was stated in [6] that it does not save power until frequencies of several megahertz.

V. Clock Network Design For Sub-vt

Though the two previous works [4][6] focus on controlling slew, skew has so far been overlooked and has only been indirectly improved with the methods above. The authors of [7] look to address this issue. Spawning from this aim, the question of suitable design of the clock network for sub-V_T circuits is discussed, and the conventional need for a buffered H-tree is scrutinized in this work.

The reason buffered trees are re-looked is because a characteristic for sub-V_T circuits is that the interconnect resistance and thus delay is negligible when compared to gate delay. Interconnect load is also much more robust to process variation. Thus, with these characteristics in mind, the authors of [7] proposed and compared an un-buffered H-tree, depicted in Fig. 5, where all registers are driven by a centralized large

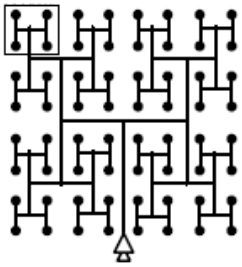

Fig. 5. [7]Un-buffered clock H-tree.

buffer. The idea is that interconnect provides path delay balance better than buffers due to the robustness to process variation. At the same nominal skew constraint, un-buffered trees exhibit an energy penalty(Fig. 6(a)), but when process variation is observed, un-buffered trees have a 4 order-of-magnitude advantage over buffered trees(Fig. 6(b)). Using such a method, the authors designed a clock tree for a version of the MSP 430 micro-controller. Chip measurements show a skew improvement of 36× over the base case(buffered clock tree) considering process variation. This leads us to believe that clock tree design methodology should be radically different in sub-V_T.

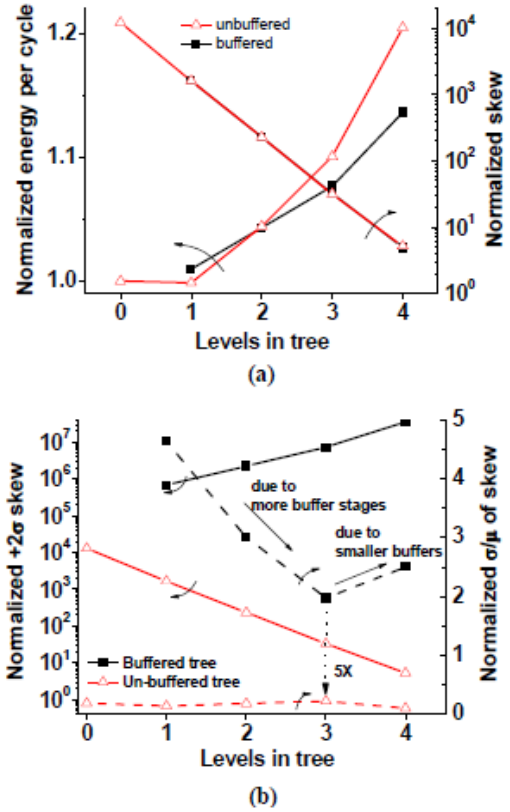

Fig. 6. [7](a) Energy penalty using centralized buffer for the same skew constraint. (b) Un-buffered trees exhibit 4 orders of magnitude skew robustness to process variation.

VI. Conclusion

The problem of clock network design in the sub-threshold regime has been introduced, and several proposed solutions have been presented. A breadth-wise observation from these different solutions tells us that a method will exhibit several tradeoffs, and that not all metrics such as power, slew, and skew will be optimal. Therefore, the notion that a universal solution is not imminent should be kept in mind.

VII. References

[1] G. Yang, Ed. “Body Sensor Networks,” *Springer*, 2006.
[2] B. H. Calhoun., A. Wang, N. Verma, A. P. Chandrakasan, "Sub-threshold Design: The Challenges of Minimizing Circuit Energy," International Symposium on Low Power Electronics and Design (ISLPED), pp. 366-368, October 2006.
[3] B. H. Calhoun, A. P. Chandrakasan, "Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS," IEEE ISSCC, pp. 300-301, February 2005.
[4] J. R. Tolbert, X. Zhao, S. K. Lim, S. Mukhopadhyay, “ Slew-Aware Clock Tree Design for Reliable Subthreshold Circuits”, ISLPED, August 2009.
[5] N. Magen, et al, “Interconnect power dissipation in a Microprocessor,” *Int. Workshop on SLIP*, 2004
[6] Jonggab Kil, et al, “A High-Speed Variation-Tolerant Interconnect Technique for Sub-threshold Circuits Using Capacitive Boosting,” ISLPED, 2006, pp. 67-72.
[7] Mingoo Seok, D. Blaauw, D. Sylvester, "Clock Network Design for Ultra-Low Power Applications,"International Symposium on Low Power Electronics and Design, Aug, 2010. V_{DD}